Notice of Allowability	Application No.	Applicant(s)	
	10/692,940	SEKIGUCHI, MASARU	
	Examiner	Art Unit	
	Quochien B. Vuong	2685	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *10/27/2003*.

2. ☒ The allowed claim(s) is/are *1-20*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 10/27/03, 10/18/04
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Reasons for Allowance

1. Claims 1-20 are allowed over the cited prior art.

2. The following is an examiner's statement of reasons for allowance:

Regarding independent claim 1, Aiura et al. (US 6,346,901) disclose a current cell type digital-to-analog converter (figure 1) comprising: a current cell matrix including a plurality of upper current cells and at least one lower current cell so as to form a matrix pattern; and a plurality of power supply lines (101-108) respectively provided in rows of the current cell matrix (column 3, lines 15-51). However, Aiura et al. fail to disclose the current cell type digital-to-analog converter further comprising in which all of the current cells have the same number of constant current transistors connected in parallel and the constant current transistors are the same size; an upper control circuit provided within each of the upper current ceils for outputting currents of all the constant current transistors within the upper current cell when the upper current cell is selected; at least one lower control circuit provided within each of the at least one lower current cell for outputting only current of a predetermined number of constant current transistors within the lower current cell when the lower current cell is selected; a plurality of power supply lines respectively provided in rows of the current cell matrix so that each power supply line supplies currents to the constant current transistors provided in the upper current cell and provided in the corresponding row; the lower current cell an upper decoder for selecting none or at least one of the upper control circuits in accordance with predetermined one or more upper bits of a digital value; a lower decoder for selecting none or at least one of the lower control circuits in accordance with

predetermined one or more lower bits of the digital value; and an analog output terminal for outputting a summation of output currents of the upper current cells and the at least one lower current cell.

Regarding independent claim 13, Aiura et al. disclose a current cell type digital-to-analog converter comprising: matrix means including a plurality of upper current cells and at least one lower current ceil so as to form a matrix pattern (column 3, lines 15-51). However, Aiura et al. fail to disclose the current cell type digital-to-analog converter further comprising in which all of the current cells have the same number of constant current transistors connected in parallel, and the constant current transistors are the same size; first means provided within each of the upper current cells for outputting currents of all the constant current transistors within the upper current cell when the upper current ceil is selected; at least one second means provided within each of the at least one lower current cell for outputting only current of a predetermined number of constant current transistors within the lower current cell when the lower current cell is selected; a plurality of third means respectively provided in rows of the matrix means so that each third means supplies currents to the constant current transistors provided in the upper current cell and the lower current cell provided in the corresponding row; fourth means for selecting none or at least one of the first means in accordance with predetermined one or more upper bits of a digital value; fifth means for selecting none or at least one of the second means in accordance with predetermined one or more lower bits of the digital value; and sixth means for outputting a summation of output currents of the upper current cells and the at least one lower current cell.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

4. The information disclosure statements (IDS) submitted on 10/27/2003 and 10/18/2004 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ogawara (US 5,162,800) discloses digital-to-analog converting unit with improved linearity.

Hori et al. (US 5,574,455) disclose digital to analog converter and frequency synthesizer using the converter.

Mori (US 6,275,179) discloses digital to analog converter using a current matrix system.

Kinugasa (US 6,683,549) discloses digital-to-analog converter.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quochien B. Vuong whose telephone number is (571) 272-7902. The examiner can normally be reached on M-F 9:30-18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on (571) 272-7899. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QUOCHIEN B. VUONG
PRIMARY EXAMINER

Quochien B. Vuong
Feb. 04, 2006.